Design of Robust, Low-Power CMOS Circuits for Millimeter-Scale Sensor Nodes

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***Abstract*—Design techniques for robust, low-power CMOS circuits are presented for applications in wireless cubic-millimeter sensor nodes. First, the design of a two-transistor voltage reference is described and its characteristics simulated. Then, a low-voltage toggle flip-flop circuit is discussed and modeled using standard switching theory. Finally, a study of the battery used to power the cubic-millimeter system is detailed.**

***Index Terms*—Low-power circuit design; voltage references; sequential circuits; logic optimization; solid-state batteries**

I. Introduction

RAPID advances in semiconductor process technologies during the course of the past several decades have spurred the development of micro- and nano-electronic devices of unprecedented complexity, capability, and versatility. Although consumer-grade microprocessors have garnered much of the attention paid to the integrated circuits industry in recent years, aggressive device scaling has led to an increase in the prevalence of wireless and mobile devices, thereby marking the beginning development of a vast new application space for integrated circuit design. One particular discipline that has begun to emerge from this new application space concerns a subject referred to as ubiquitous computing. At present, vast amounts of valuable data remain uncollected due largely to the absence of sensors of sufficient efficacy and integration density. For example, the activities of pathogens and other foreign agents in the body remain essentially unmonitored outside the office of a physician, as devices possessing adequate lifetimes and minimally invasive implantation techniques do not presently exist. It is therefore the objective of the discipline of ubiquitous computing to develop a means of efficiently disseminating sensors in all manner of locations. Recent work by the Blaauw Research Group at the University of Michigan Department of Electrical Engineering and Computer Science has led to the development of an integrated sensor of cubic-millimeter (mm^3) dimensions [1]. Termed the Michigan Micro-Mote (M^3), the device possesses a number of standard features, including a processing unit, memory, and a radio, as well as several specialized features, such as sensors of various types, a sophisticated power management unit, and a variety of energy-harvesting peripherals. In order to realize such a low-power system, specialized circuit design techniques must be utilized. This work details a number of design considerations that may be applied to implementation of an ultra-low-power system. A brief discussion of the methods used to characterize the battery powering system is also included.

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II. Design of Low-Power Voltage References

The vast majority of analog circuits require at least one constant voltage reference in order to implement a desired function. While a wide array of voltage references is available in the published literature, most of these circuits consume power on the order of microwatts and require large, often complex amplifiers for stability [2]. Moreover, many of these designs require the use of integrated resistors, which are known to be large and highly sensitive to variations in the manufacturing process. A two-transistor voltage reference that achieves picowatt power consumption without the use of amplifiers and integrated resistors was presented in [2]. Variations on this design will be discussed in the following subsections.

A. 2T Voltage Reference Designs

The two-transistor (2T) voltage reference originally described in [2] is shown in Fig. 1. The circuit consists of a native NMOS transistor, the gate of which is tied to ground and the drain of which is connected to the power supply, and a thick-oxide I/O diode-connected NMOS device, the source of which is tied to ground. Connecting the gate of the upper device to ground induces the transistor to operate in the subthreshold region, which ensures that the device draws a very small current from the supply. While subthreshold operation is known to enable ultra-low-power design, the small current level associated with subthreshold conduction dramatically increases the susceptibility of a circuit to process, voltage, and temperature (PVT) variations [3]. Compensation for these effects will be considered in the succeeding subsection.

Fig. 2 presents a second implementation of the two-transistor voltage reference [4]. In this circuit, the lower NMOS device has been replaced with a diode-connected PMOS transistor. The PMOS-based circuit can be further adapted to provide several reference voltages by increasing the number of diode-connected devices, as shown in Fig. 3.

B. Circuit Analysis and PVT Compensation Schemes

An examination of the effects of PVT variations on the circuits here presented begins with writing the current-voltage equations for each transistor. For the two-transistor stacks, the

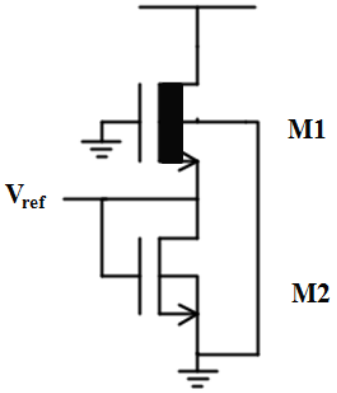
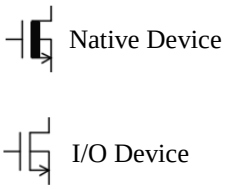


Figure 1: The NMOS-based 2T voltage reference presented in [2].



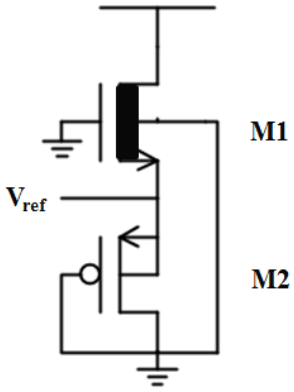


Figure 2: The PMOS-based 2T voltage.

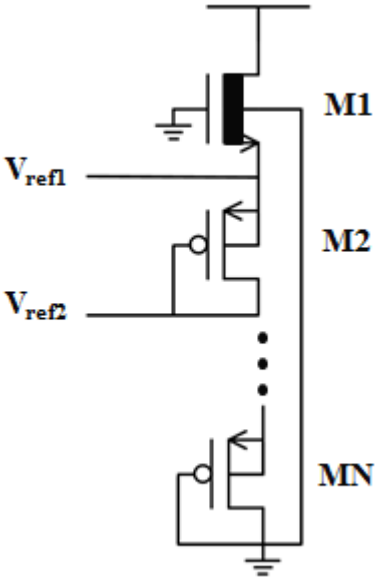


Figure 3: A voltage reference with multiple output voltages obtained from the 2T design by increasing the number of diode-connected devices [4].

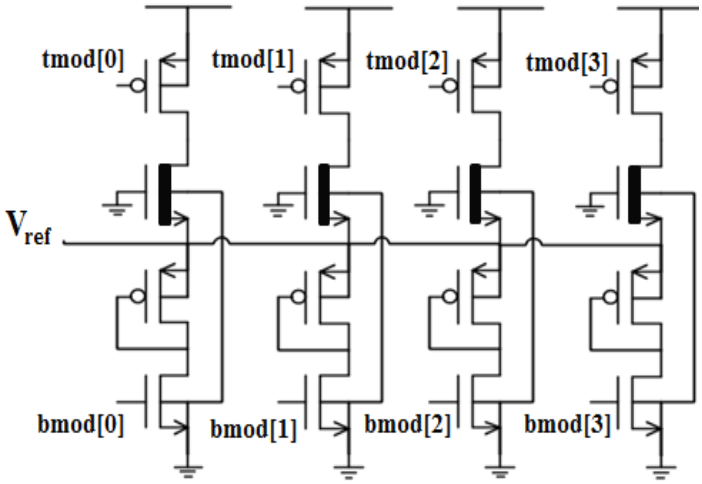


Figure 4: The tuning circuit used for post-fabrication modification of the output voltage. The switches may be rendered active by applying the appropriate control signals; any combination of *tmod[0:3]* or *bmod[0:3]* may be used [2].

analysis is nearly identical for the NMOS and PMOS designs. Hand-analysis quickly becomes intractable for a large number of diode-connected devices, so the two-transistor configuration will be considered only; the PMOS design is chosen for analysis. For a transistor operating in the subthreshold region, the current-voltage relationship is given as [5]:

$$I_{sub} = \mu C_{ox} \frac{W}{L}(m-1)\phi_T^2 \exp\left(\frac{V_{gs}-V_{th}}{m\phi_T}\right)\left(1-\exp\left(\frac{-V_{ds}}{\phi_T}\right)\right) \quad (1)$$

Here, μ is the carrier mobility, C_{ox} is the oxide capacitance, W is the transistor width, L is the gate length, m is the subthreshold slope factor, ϕ_T is the thermal voltage, V_{gs} is the gate-to-source voltage of the transistor, V_{th} is the transistor threshold voltage, and V_{ds} is the drain-to-source voltage of the transistor. For the NMOS device, the current equation may be written as:

$$I_n = \mu_n C_{ox,n} \frac{W_n}{L_n}(m_n-1)\phi_T^2 \exp\left(\frac{-V_{ref}-V_{th,n}}{m_n\phi_T}\right) * \left(1-\exp\left(\frac{-(V_{DD}-V_{ref})}{\phi_T}\right)\right) \quad (2)$$

Here, V_{ref} is the output voltage and $V_{DD}$is the supply voltage. Similarly, for the PMOS device:

$$I_n = \mu_p C_{ox,p} \frac{W_p}{L_p}(m_p-1)\phi_T^2 \exp\left(\frac{V_{ref}-V_{th,p}}{m_n\phi_T}\right) * \left(1-\exp\left(\frac{-V_{ref}}{\phi_T}\right)\right) \quad (3)$$

Equating (2) and (3) and solving for the reference voltage yields:

$$V_{ref} = \frac{m_1 m_2}{m_1+m_2}\left[(V_{th,p}-V_{th,n}) + \phi_T \ln\left(\frac{\mu_n C_{ox,n} W_n L_p}{\mu_p C_{ox,p} W_p L_n}\right)\right] \quad (4)$$

The relation given by (4) reveals that, to first-order, the reference voltage is independent of the supply voltage; thus, the circuit should be robust to voltage variations. The extent to which a circuit is sensitive to supply variations is defined by a metric referred to as the line-sensitivity (LS); the LS is defined as:

$$LS = \frac{\frac{\max(V_{ref}) - V_{ref}(\Delta S = 0.01 * S_{nom})}{\max(V_{ref})}}{V_{DD,max} - V_{DD,min}} \quad (5)$$

Here, S is the slope of the reference voltage-supply voltage plot and S_{nom} is the nominal slope.

A corresponding metric for the sensitivity of the reference voltage to the ambient temperature is the temperature coefficient (TC). The TC is defined as [2]:

$$TC = \frac{\frac{\max(V_{ref}) - \min(V_{ref})}{V_{ref}(T = 20\,^0C)}}{(T_{Max} - T_{Min})} \quad (6)$$

Here, T is the ambient temperature. It will be assumed that the subthrehold slope factors, mobility, and oxide capacitance are, to first-order, independent of temperature. The thermal voltage is given as $\phi_T = k_B T/q$, where k_B is the Boltzmann constant and q is the elementary charge. The threshold voltage temperature dependence will be modeled by a simple linear relation, given as $V_{th} = V_{th}(T_0) - C(T - T_0)$ [6], where T_0 a reference temperature and C is a constant. Differentiating (4) with respect to temperature produces:

$$\frac{\partial V_{ref}}{\partial T} = \frac{m_n m_p}{m_n + m_p}\left[(C_p - C_n) + \frac{k_B}{q}\ln\left(\frac{\mu_n C_{ox,n} W_n L_p}{\mu_p C_{ox,p} W_p L_n}\right)\right] \quad (6)$$

From (6), it may be seen that the temperature dependence of the output voltage depends on the process constants, as well as the device dimensions. A circuit designer rarely exercises much control over the fabrication process, so compensating the circuit for temperature variations must be accomplished by selecting the appropriate device sizes. Equating (6) to zero and solving for the ratio of the transistor widths gives:

$$\frac{W_n}{W_p} = \frac{\mu_p C_{ox,p} L_p}{\mu_n C_{ox,n} L_n}\left(\frac{q}{k_B}(C_p - C_n)\right) \quad (7)$$

The result given by (7) indicates that the temperature dependence of the output voltage may be reduced to zero by properly selecting the ratio of the device widths. A strategy for choosing the required widths will be discussed in the following subsection.

Relation (4) also provides insight into the dependence of the output voltage on the process parameters. The presence of the natural logarithm in (4) serves to suppress the effects of variations in the carrier mobilities, oxide capacitances, and device dimensions. Furthermore, the reference voltage depends on the difference of the threshold voltages, rather than on the absolute values of these parameters. If the silicon layout for the devices is done carefully, the variations in the threshold voltages should approximately track each other, thereby producing a minimal effect on the reference voltage. Thus, the circuit provides an innate resilience to process variation.

From the foregoing discussion, it would seem that the 2T voltage references should perform almost precisely as expected once integrated into a circuit of interest. However, the equations used to model the behavior of the voltage references are accurate to first-order only and do not consider secondary effects that occur due to random variations in the manufacturing process and silicon layout dependencies. Although these secondary effects may be mitigated by utilizing the techniques described above, it is often desirable to include circuitry for post-fabrication tuning of the voltage reference; such a circuit is shown in Fig. 4 [2]. Four 2T

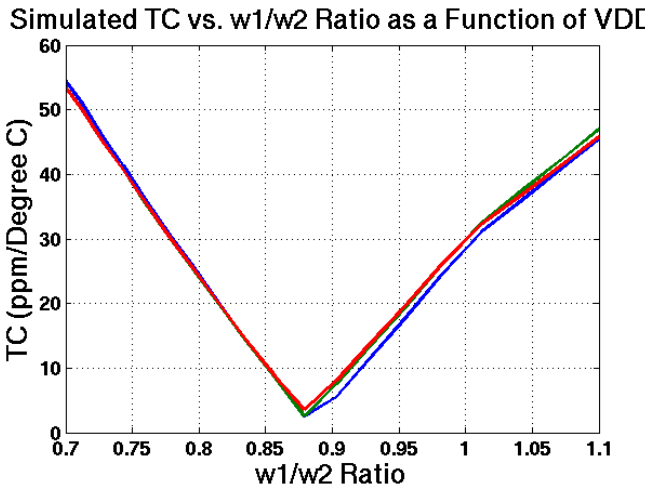


Figure 5: Simulation results used to select the optimal device width ratio. The plot shown here is for the 2T NMOS configuration.

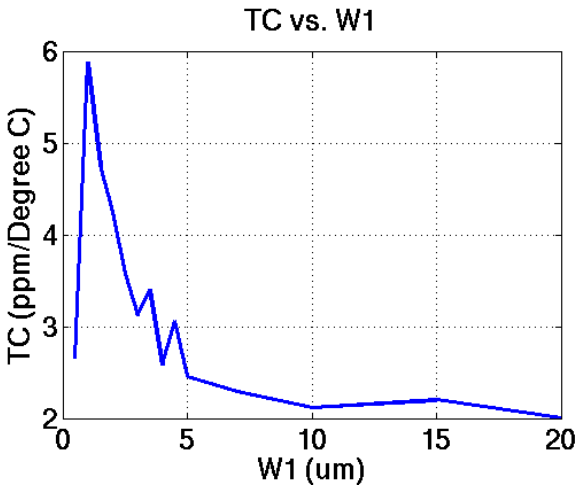


Figure 6: Plot of the optimal temperature coefficient for a fixed W_2 with W_1 varied. The simulation results are for the 2T NMOS reference.

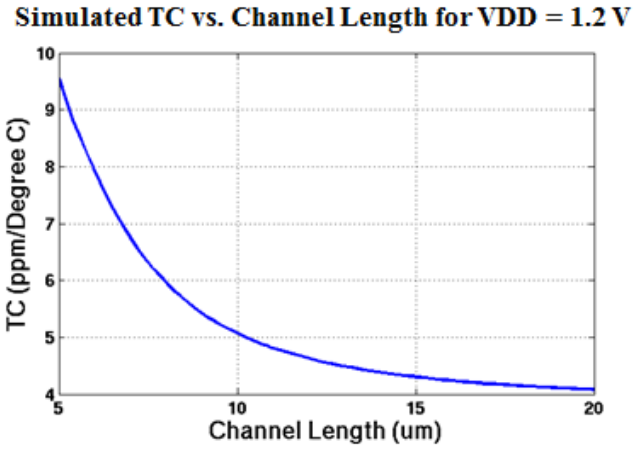


Figure 7: Result of sweeping the transistor gate lengths of the 2T NMOS reference. The gate lengths of the two devices are assumed to be equivalent.

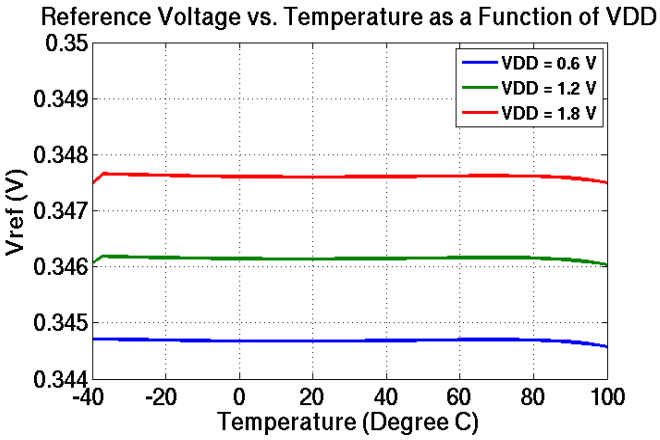


Figure 8: Demonstration of the insensitivity of the reference voltage to temperature and voltage variations when the proper device ratio is selected for the 2T NMOS design.

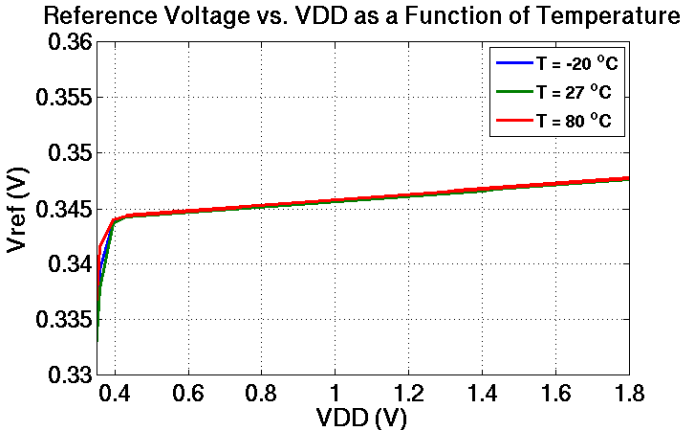


Figure 9: Further demonstration of the insensitivity of the output voltage to temperature and voltage variations for the 2T NMOS configuration.

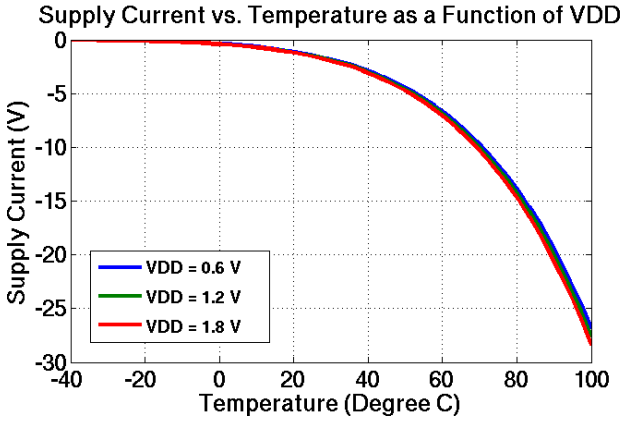


Figure 10: Current draw of the 2T NMOS reference used to calculate the power consumption.

voltage references are connected by a common output line and each reference possesses two additional transistors that behave as switches. When the switches are active, the corresponding reference transistors influence the output voltage; when the switches are inactive, the corresponding reference transistors produce a negligible impact on the output voltage. The tuning circuit may be used to modify the width ratio of the top and bottom transistors in Fig. 2 to compensate for the effects of PVT variations on the output voltage.

C. Simulation Results

Fabrication of a chip is often completed in a series of steps; this procedure is referred to as the design flow. The design flow begins when a designer conceives an idea for a circuit on paper. To test the idea, the designer will then utilize a commercial circuit simulator; standard commercial simulators include Spectre and HSPICE.

In the present case, the circuit has already been drawn, so the task that remains in the design phase is the sizing of the devices. Sizing of the devices was accomplished by fixing the size of the lower transistor in the 2T stack and conducting a parametric sweep of the upper transistor width in order to determine the optimal device width ratio; the results of the sweep are shown in Fig. 5. With the proper ratio obtained, the absolute device widths were optimized by fixing the lower transistor width and sweeping the upper transistor width, as shown in Fig. 6. Additionally, the lengths of the devices were swept in order to find the gate length that produces the smallest TC with the lowest power consumption; the result of this study is shown in Fig. 7. Fig. 8 and 9 show the results of sweeping the temperature and supply voltage and Fig. 10 shows the current draw of the 2T voltage reference.

D. Implementation in Silicon

Completion of exhaustive simulations marks the end of the initial design phase and the beginning of the layout and verification phases. Concrete realization of an integrated circuit is achieved by implementing the circuit in silicon, which is done by completing the layout of the transistors, input and output (I/O) pads, and discrete components. The small size of the present chip necessitates the use of a simplified variant of chip-level layout. The procedure is as follows. First, the layout for the individual blocks is done; for the chip here considered, the blocks are the individual voltage reference test structures. Once the blocks are completed, each unit is placed in the top-level layout, which contains, in addition to the blocks, components for the I/O pads and crack-stop; the crack-stop is simply a stack of metal that is placed along the perimeter of the chip to prevent the underlying silicon from splitting when the chips are diced. Metal wires are then used to route from the placed blocks to the I/O pads. Verification of connectivity is performed after routing by simulating the top-level chip using a fast circuit simulator, such as FineSim or Analog Fast Spice (AFS).

The voltage reference test chip was designed in 180nm CMOS technology using a standard commercial process. An image of the final chip-level layout is given in Fig. 11 and the corresponding floor-plan is given in Fig. 12. The layout shown represents the form of the chip as it will appear after fabrication. Currently, the chip is in production and is expected to return for testing in late August 2014.

III. Design of a Low-Voltage Toggle Flip-Flop

Just as voltage references are ubiquitous in analog designs, sequential elements are pervasive in digital designs. A common sequential element is a one-bit register, termed a flip-flop, which may store a Boolean value of either zero or one. In addition to functioning as memory devices, flip-flops may also be configured to behave as toggle elements, which are devices that invert the presently stored state at the start of each clock cycle; a flip-flop designed to achieve this function is referred to as a toggle flip-flop (TFF). TFF are essential building blocks of certain varieties of binary counter circuits, which are frequently used in timing devices in many designs. Since a TFF will switch once during each clock cycle, it will draw current, and therefore energy, from the supply once every cycle, in addition to the leakage currents that are drawn during inactive periods.

It is common for counter units to consume a significant portion of the logic power of a circuit. To mitigate this high power consumption, low-power systems often operate at reduced supply voltages. Many sequential circuit elements fail to operate correctly at low supply voltages, particularly when process variations are considered. Thus, it is the objective of this study to design a low-power TFF that is robust at low voltages.

A. Modeling the TFF

As is the case with all sequential elements, the functionality of a TFF may be described using a finite state machine (FSM). Assume that the output of the TFF is initially zero and that the clock input signal is also zero; label this state as *A*. If the clock transitions to a logical high value, the output of the TFF should transition to one; label this state as *B*. When the clock transitions to logical low, the TFF output should remain at one; label this state as *C*. If the clock transitions to logical one again, the TFF output should fall to zero; label this state as *D*. Finally, if the clock transitions again to logical zero, the output of the TFF should remain at zero and the FSM should then return to state *A*; a diagram of the TFF FSM and its corresponding state table are shown in Fig. 13 and Table I, respectively.

Implementation of the FSM using CMOS technology may be accomplished by selecting an appropriate encoding for the various states and composing the excitation equations that describe the machine. Choosing the proper encoding, however, is often a difficult task [7].

To analyze the state machine, let *S* be defined as a set, the elements of which are the states of the machine *M*. Each state encoding corresponds to a pair of partitions, one for each state variable, of the set *S* [8].

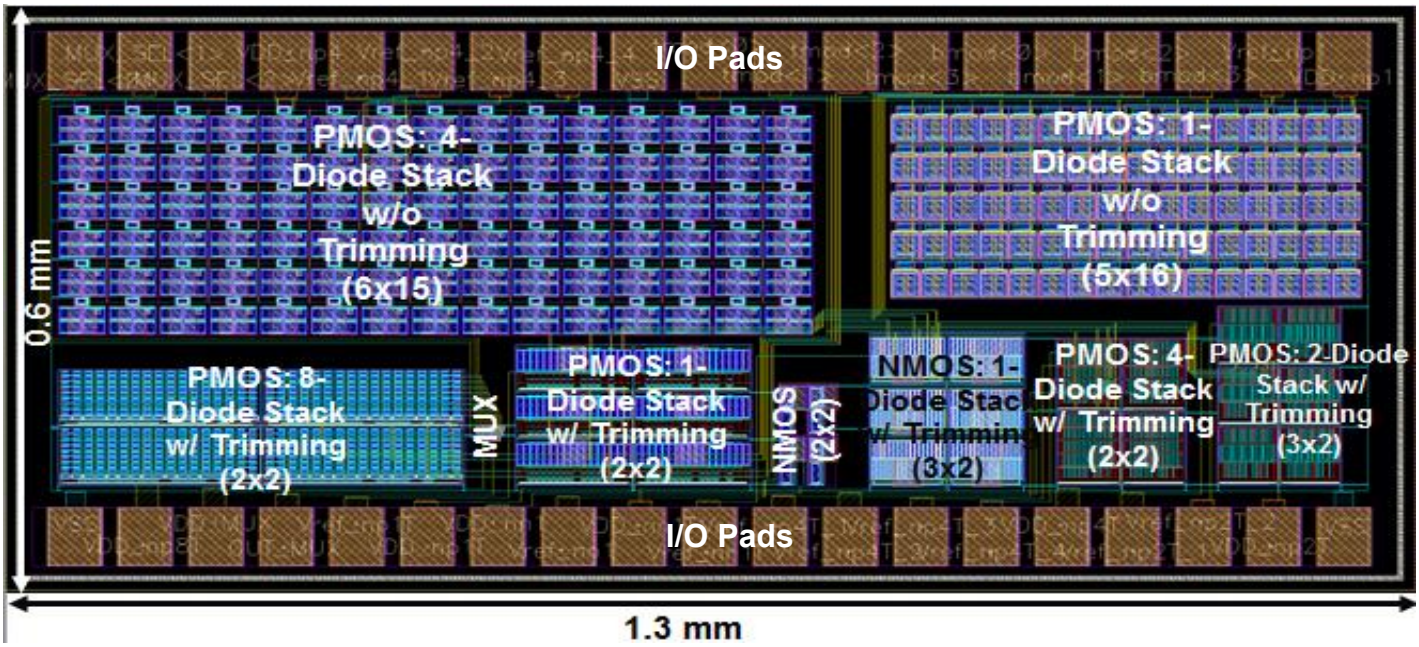


Figure 11: Top-level silicon layout of the voltage reference test chip.

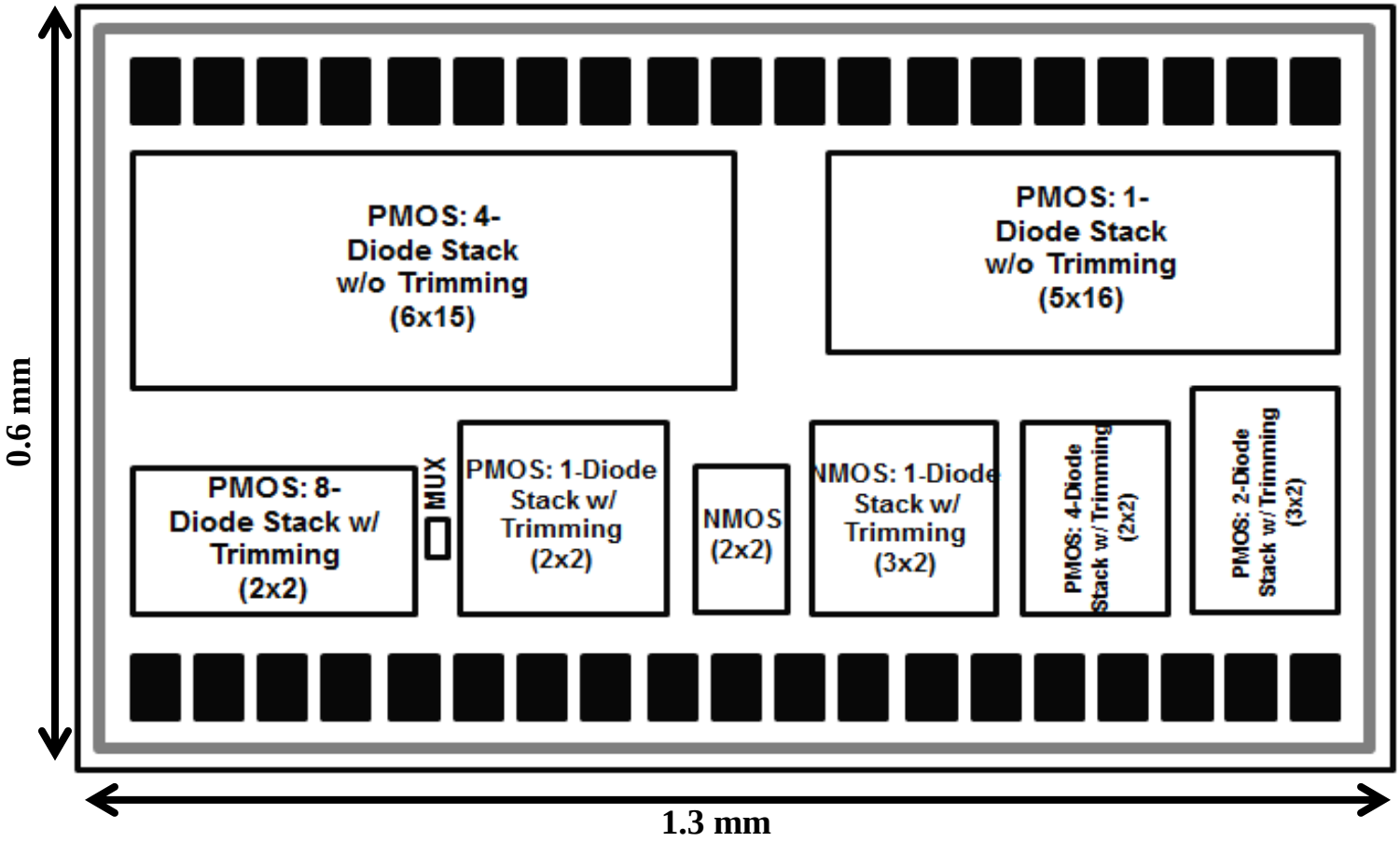


Figure 12: Floor-plan of the final chip-level layout.

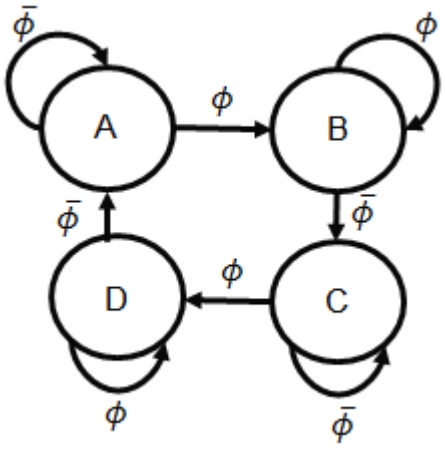


Figure 13: Finite state machine for the toggle flip-flop. The symbol ϕ is the clock input and an over-bar denotes the logical complement.

TABLE I
STATE TABLE FOR TOGGLE FLIP-FLOP

Previous State	Next State 0	Next State 1	Output
A	A	B	0
B	C	B	1
C	C	D	1
D	A	D	0

For the machine *M*, robustness is achieved by ensuring that race conditions and glitching are avoided during state transitions; this requirement reduces the probability that the sequential element will enter into an incorrect state after a transition. Such a constraint may be applied to *M* by selecting a state encoding such that the partitions of *S* permit a single state variable to switch during each state transition [7, 8]. Such a method was successfully implemented in [9] and will therefore be adopted here.

B. *Implementation of the Toggle Flip-Flop State Machine*

Concrete implementation of the TFF machine may be performed in a variety of manners. The simplest approach is to begin with a D-type flip-flop and connect the complement of the flip-flop output to the input of the flip-flop. If this approach is utilized, the efficiency and robustness of the design will depend strictly on the choice of flip-flop. An exceedingly large number of flip-flop designs exist within the published literature [9-13], each of which offers certain advantages and disadvantages. As part of the present study, a number of these existing designs were analyzed and compared with several proposed designs.

Another approach to designing a TFF is to implement the excitation equations derived in the preceding subsection using conventional Boolean gates, then using a topological-compression technique to reduce the circuit size and clock loading [14]. This method, while simple and effective at reducing the circuit area, may result in reduced robustness due to the poor electrical characteristics of the resulting connections. As such, this technique was employed with caution during the present study.

Because the results of this study may be used in a future publication, further details will be omitted here for the purpose of confidentiality.

IV. SOLID-STATE BATTERY CHARACTERIZATION

Although circuit-level design is often of paramount interest when describing the implementation of a millimeter-scale system, the means by which the system is powered is tantamount to circuit design considerations. Effectively powering a mobile system within a compact form-factor is a difficult task, largely because batteries with sufficient cycle lifetimes and voltage characteristics are difficult to manufacture within a small volume. Thin-film solid-state batteries have been developed during the course of the past decade that provide reasonably stable output voltages within a small form-factor. However, the cycle lifetimes of these batteries are often of concern, particularly if a system is required to operate for many years with a single battery. Thus, the subject of the present study is to examine the charge and discharge behaviors of a commercially available solid-state battery and evaluate the performance with respect to cycle lifetime.

A. *Description of Measurement Setup*

The design of the M^3 sensor node is such that the system draws a current for a short duration, then enters a dormant mode during which energy is harvested from the ambient environment to charge the battery. Thus, the measurement procedure was configured to emulate this duty-cycled charge-discharge sequence. As a specific example, one of the tests conducted consisted of an initialization period, during which time the battery was charged to its full voltage, followed by a continuous sequence of alternating 500ms discharge and 10s charge intervals; the charge and discharge currents were chosen to approximate those existing in the implemented system.

Selection of the charge and discharge times and currents directly affects the lifetime of the battery. If the charge and discharge cycles are properly balanced, then the output voltage of the battery will remain relatively stable over a large number of charge and discharge cycles. It is often the case, however, that the times and currents required to achieve a balance between the charge and discharge cycles are not known prior to testing. Thus, it was necessary to implement a simple control algorithm to adaptively tune the charge current to balance the discharge cycle for a given charge time, discharge time, and discharge current. Fig. 14 provides a block diagram of the implemented control algorithm. After the battery is fully

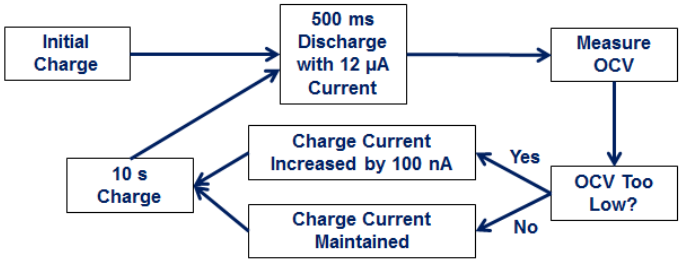


Figure 14: Block diagram of the control algorithm used to adaptively tune the battery measurement setup.

charged at the beginning of the test, the previously described charge and discharge cycles are permitted to commence. When a measurement is taken, the software in which the algorithm is implemented will check the output voltage of the battery and compare the result against a pre-set threshold. If the output voltage is too low, the software will configure the source-meter that the supplies the battery to increase the charge current, while maintaining all other relevant test parameters at the currently set values.

B. *Measurement Results*

Fig. 15 provides a plot of a typical test run. Two quantities are of interest when evaluating the cycle lifetime of a battery; these quantities are the open-circuit voltage (OCV) and the loaded voltage. The OCV is the voltage measured when no external load is applied to the battery. The loaded voltage may be found by accounting for the voltage dropped across the internal resistance that is present in the battery; thus, $V_{Loaded} = V_{OC} - IR_{Internal}$. Control of the charge current is based upon the measured OCV, rather than the loaded voltage.

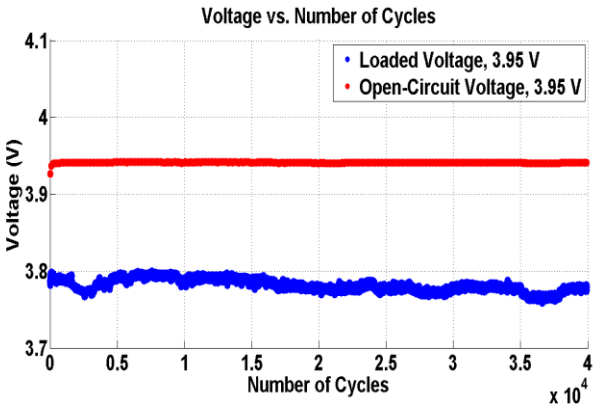


Figure 15: Battery output voltage as a function of the cycle count. The loaded voltage is derived from the open-circuit voltage by applying the relation $V_{Loaded} = V_{OC} - IR_{Internal}$.

V. Conclusion

Design techniques and circuits for applications in low-power wireless sensor nodes have been presented and preliminary results have been discussed. While numerous other methods for designing robust, low-power CMOS circuits exist, the approaches here described constitute a good first sampling of the available techniques. Future work will seek to further characterize these circuits by in-lab testing and additional simulations. In particular, the voltage reference test chip will be measured and the results will be compared with the simulations. The toggle flip-flop circuit will be further studied and a final design may be fabricated and tested. Measurement of the solid-state battery characteristics will continue.

Acknowledgement

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