DESIGN OF A LOW-CURRENT VOLTAGE DIVIDERS

A Summer Research Final Report

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By

Shiming Song

Undergraduate Student,

Department of Electrical Engineering and Computer Science,

University of Michigan

Faculty Advisor: Professor David Blaauw

Graduate Student Advisor: Yenpo Chen

0. Abstract

Situations abound in integrated circuits design where a voltage level different from the power supply voltage is needed. A traditional way to obtain a lower voltage is to use a resistor-in-series voltage divider. This design provides reference voltage values with desirable accuracy and is also robust to temperature change and manufacturing variation. However, this design has a significant steady state current in the circuit and the current can be very wasteful of power in low current VLSI design. The only way to lower the current is to enlarge the resistance area but the over-size problem, in turn, can also be substantial.

The main goal of my research in summer, 2011 is to solve this current-area dilemma in creating a low-voltage reference node. This report briefly summarizes my main findings and results. More details on the problems of resistor-in-series design are included. Three alternative designs, off-state MOS, diode-connected switches, and switched-capacitor circuits will be discussed and their respective simulation results will be provided and analyzed. All the designs included in this report are implemented, tested, and analyzed on the simulation level using commercial design software and models.

Table of Content

I. Introduction

It is common for some components in VLSI design to require a different operating voltage. But the entire system is usually powered by only one supply with one fixed voltage. Therefore extra circuits are needed to convert the supply voltage to a different, usually lower, voltage level, in order to guarantee correct functionality. A most intuitive design of this converter is to borrow the widely accepted voltage divider in traditional classroom circuit design. This design involves several identical resistors connected in series between VDD and ground of the power supply (figure 1). Voltage distributes evenly on the resistors and we can hence obtain the desired output level by outputting voltage from the right node.

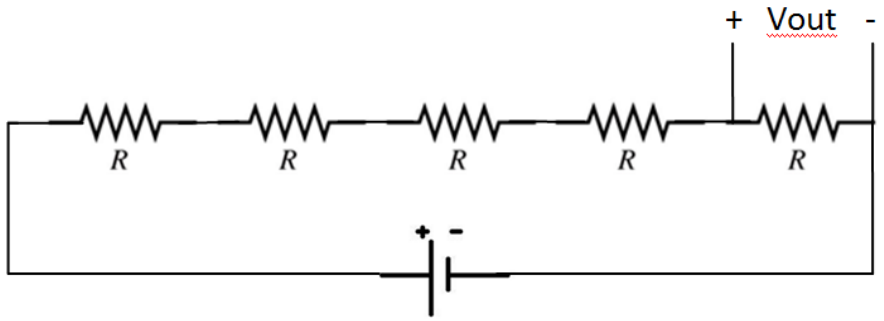

Figure 1: An example traditional divide-by-5 voltage divider

The advantages of the traditional design include good stability, accuracy, and robustness in some sense that will be defined in later sections. However, a substantial weakness in this design is that there is a finite resistance between the anode and the cathode of the power supply and therefore a significant steady state current keeps flowing throughout the operations. This is not desirable because a normally sized design can easily yield a current millions times higher than the main part of a low current design. The steady state current can be reduced by adding more resistance to the circuit. But this introduces extra area that might double the size of the whole system, which is apparently not desirable, either.

There is not much flexibility in the area-current tradeoff in the traditional design because of the extreme simplicity. Other approaches are hence needed.

Three alternative designs will be discussed and compared on simulation in the following sections. The designs are off-state MOS, which uses off-state MOSFETs in the place of resistors to lower the current, diode-connected switches which involves an array of on-state switches to divide the current at the same time with voltage, and switched capacitor circuit which uses capacitors to move charge so that steady state current is eliminated.

All the four designs were simulated using commercial software and models. The results are compared in this report and analysis based on the results follows.

II. Overview

Before we look into the simulation results, this section gives a brief overview into each design. Background theories and design methodologies will be discussed. Also, some first order analysis and rough prediction of the design's behavior under different conditions will be provided.

A. Resistor in Series Design

This design is the traditional approach. The circuit involves several resistors put in series between VDD and ground of the power supply. An example divde-by-5 circuit diagram was shown in "Section I: Introduction."

The theory behind this design is simple. When several identical resistors are connected in series, the total voltage evenly distribute on them and we can thus simply output the desired voltage level by probing at the right node. In addition, in order to control the current within acceptable range, the resistors have to be sized up substantially.

The advantages of this design are accuracy and robustness. It yields an accurate output because the circuit operates in DC condition and no switching is involved. So the output will not be affected by sources other than environment noise.

It is robust in two ways. First, in respect of manufacturing variation, usually the bigger the devices are, the less likely the circuit will be affected by variations. In this design, the resistors have to be oversized to overcome the power waste through steady state current. Therefore, the huge area in some sense protects this design from variation very effectively. Second, the resistors are made of less conductive materials with much lower doping level. So the change in temperature will not affect the current significantly.

The disadvantage of this design is the extremely big area. In low current design, we usually expect the voltage divider to draw pico-amp (10^{-12}) range current. Thus the design involves several hundreds of giga-ohm (10^{9}) of resistance. The resistance of this size, in turn, will occupy an area that can be enough for some smaller complete systems.

B. Off-state MOSFET Design

This design is very similar to Resistor-in-Series except that we are using off-state MOSFETs instead of real resistors. MOSFET is short for Metal-Oxide-Semiconductor Field Effect Transistor. The structure of a MOSFET roughly involves a piece of silicon-dioxide(insulator) sandwiched between a piece of polysilicon(conductor) and a piece of silicon(semiconductor). Two nodes on the silicon, called "source" and "drain", are built and used to connect to the outside circuit. In addition, the polysilicon part is also connected to other circuitry and usually referred to as "gate." And there are usually two voltages defined for the gate, "on voltage" and "off voltage". When the gate is at off-voltage, the resistance

between the source and drain is around 1G-ohm range, which makes the structure act like an insulator. But if we apply the gate voltage to the on voltage value, carriers will accumulate on the border between the oxide and silicon to form a conducting channel between source and drain and therefore the device becomes a conductor. Because of this property, MOSFETs are usually used as switches in digital integrated circuit design.

However, in this design of voltage dividers, we are keeping this switch “off”. As mentioned above, at off-state, the resistance between source and drain is around G-ohms, which is ideal to meet our current requirement. Also, if we size and bias the devices identically, they will divide the voltage equally as well. This is the motivation of this design. The diagram looks as follows.

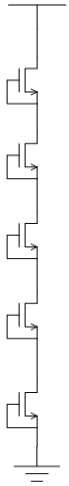

Figure 2: An example off-state-MOS divide-by-5 voltage divider

The off-state-MOS design is much smaller than the traditional resistor design. It occupies only around 0.01% of the area which would have been taken by the huge resistors. However, as will be shown in Section III B, this design is very sensitive to variation because it affects the ratio of the voltage values among the resistors. This problem is even worse when the temperature is higher. In particular, the circuit starts to fail at 100 C, which is not even a worst-case estimation of the reality condition.

Nonetheless, we can still improve the robustness by just connecting the MOSFETs differently, which brings up the next design, Diode-Connected MOSFET circuit.

C. Diode-Connected MOSFET Design

The Off-State-MOS design is very sensitive to variation because the number of MOSFETs involved is small. In a dividing-by-5 design, for example, only 5 MOSFETs are put in series and a manufacture mismatch at one of them will cause a significant distortion at the output.

However, the problem in the Off-State-MOS design can be solved simply by putting more MOSFETs in series so that the variation, which is almost completely random, will compensate and balance each other. Also, in this design the MOSFETs have to be always on instead of off, because the MOSFETs at the bottom of the stack(or series) will have a very low voltage across and hence limit the current of the

whole circuit. When the MOSFETs are configured to be always on, they are usually called “diode-connected” and thus comes the name of this design. An example diagram is shown below.

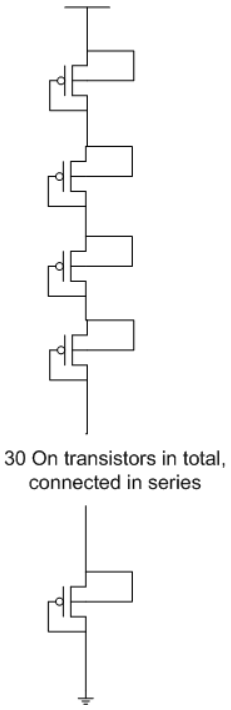

Figure 3: An example diode-connected voltage divider

As shown in the diagram, the MOSFETs actually have 4 nodes. The additional one besides the 3 we have already discussed is “body”, which leads to the silicon substrate. Body nodes are usually connected to either global VDD or VSS, based on the types of MOSFETs, and thus it is usually omitted in the diagram unless it has to be otherwise connected. In this design, all the bodies of the transistors are connected to their source nodes, so that all the MOSFETs have identical bias conditions and hence the voltage divides evenly.

D. Switched Capacitor Design

The last design studied in my research is Switched-Capacitor(SC) circuit. It is a technique widely used in signal processing circuits and some of the DC-DC converters. In our design, we are taking advantage of the open circuit nature of capacitors to obtain very low current and thus save the power.

A switched-capacitor circuit involves big capacitors connected with frequently switching components. Capacitors serve as the containers of charge and by switching back and forth among two or three connection patterns, we can manipulate the charge flow, the current.

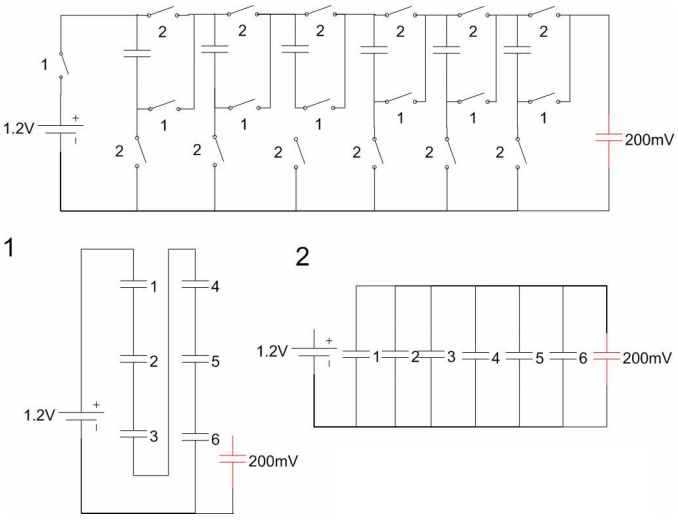

Figure 4: An example SC divide-by-6 voltage divider

The diagram above is an example switched capacitor circuit that divides the source voltage by 6. The black capacitors are the ones that are involved in switching, and they are all identical. The red one is called a “DeCap”, which is just used to stabilize the output. The DeCap is usually slightly bigger than the other capacitors. As we can see on the diagram, the switches are in two groups, Group 1 and Group 2. The two groups of switches cannot be on at the same time because otherwise they form a short circuit.

The two groups of switches take turns to be on and change the topology of the capacitor connection, as shown in Figure 4. When all the switches in Group 1 are on, the whole circuit is at Stage 1, where the capacitors are in series. The voltage distributes evenly among the black capacitors, making each of the capacitor hold 1/6 of the source voltage between there two nodes. Since capacitors are not conductive, there is essentially zero steady state current at Stage 1. To enter Stage 2, all Group 1 switches are turned off, and Group 2 switches take over. At Stage 2, all the black capacitors are connected in parallel and collaborate to charge up the DeCap, making it eventually converge to 1/6 of the source voltage.

The circuit consumes some current at the beginning to charge up all the capacitors. However, once the output is stabilized at the target voltage, the only consumption will be the leakage, which is not substantial. The whole circuit still has to switch after the output is stabilized so that the deviation from target caused by noise and leakage can be constantly fixed.

A defining advantage of this design is that the current is tunable. Based on the magnitude of power delivered at the output, we can limit the current to just the value needed by tuning the switching frequency. When load is present, the circuit usually has to switch at the frequency of several kilo-Hz, but to compare with other designs, which do not provide any power, we suppose no explicit load is to put at the output node. Therefore, the only loss of charge we are assuming in the experiment is through leakage and hence the frequency can be reduced to below 10Hz.

Still, there exist some disadvantages in this design. First, to maintain good functionality, the capacitors have to be big. This makes the circuit not as competitive in respect of area. Also, groups of switches are

involved in this design and they switch almost exactly at the same time. This can be modeled as a giant capacitor charging and discharging very fast. The switching will hence introduce an instantaneous spike of coupling current. The first problem is the generic disadvantage and can only be improved rather than solved. The second one can be eliminated with techniques introduced in *Section IV: Future Work*.

III. Testing Results

This section provides and discusses experiment results and findings. Further detailed analysis and insight in the design perspective will be provided.

The criteria we rely on to compare the designs include current level, output accuracy, estimated area and robustness.

Current level is the average current the designs draw from the main source. The output accuracy is how close the output stays from the target voltage. This is especially important for switched-capacitor design, where the output is oscillating. The estimated area is just a measurement of the size of the actual circuit.

The robustness is how much the system is immune to variation. Since the manufacture process is not exact, the design has to be able to withstand some mismatch with the design spec. In the experiment, we are modeling the random device variation using Monte Carlo sampling simulation.

In addition, the circuit has to be robust to temperature change. Especially, at high temperature, the overall performance and the current level should not change too much. Otherwise the design is not practical enough.

A. Resistor in Series Design

Experiment shows that resistor-in-series design is still the most reliable one compared to others but it is really too huge to be implemented.

The current level is tunable and depends on the resistance. To balance between the design requirement value and simulation workload, the target current is set to around 100 pA, which dictates that around 10 G-ohm resistance is present in the circuit.

This design does not have any difficulty stabilizing the output at the target voltage, the output is always a flat line at the output, as shown below.

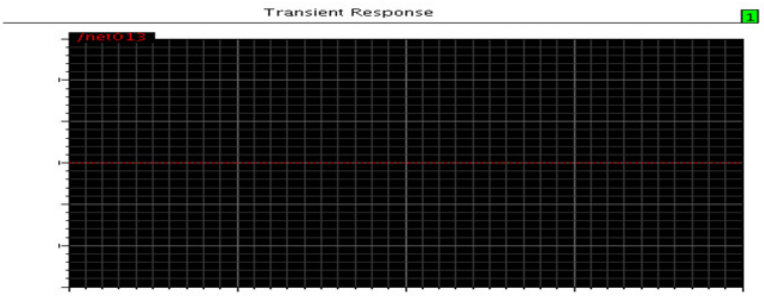

Figure 5: An example resistor-in-series output waveform

The area of the version with several hundreds of pico-Ampere is around 10mm^2, which is extremely far from desirable. This area is around 1000 times bigger than the maximum we can accept. This is the deciding disadvantage, which makes this design not worth realizing.

Monte Carlo simulation shows that this design is extremely robust to variation. This is not surprising because the area of a single component is in the millimeter squared range, which lies perfectly in the scope of the current technology. Below is an example plot of the Monte Carlo distribution of the output.

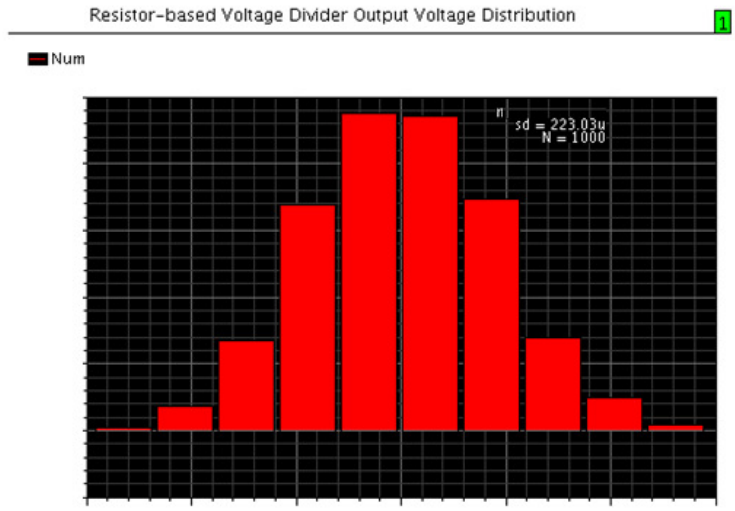

Figure 6: An example output Monte Carlo distribution

The axes were deleted to protect the lab technology but the only number we really need for the analysis is the standard deviation of the distribution. The standard deviation, also called sigma, represents how accurate the manufacture process can produce the design massively. The lower the sigma is, the higher the productivity is. In the traditional resistor-in-series design, the sigma is usually below 100uV.

Simulations at 100 C and 27 C of temperature exhibit very close results. Therefore the performance of this design is not temperature dependent. The reason behind is not complex. The resistance goes up when temperature rises and the current is thus lowered. As long as the current stays low, the circuit will be under perfect control and therefore the performance is not much affected. This is very valuable because all other designs more or less have the problem with temperature change.

B. Off-state MOSFET Design

Off-state MOSFET Design is much smaller and the current is only at the order of leakage magnitude. Also, it is easier to implement, in the sense of both design and manufacture. All these features are desirable but this design has some problem as well, some are so severe that the circuit occasionally starts to fail.

The current level of this design can reach below 1pA, which is only 1/100 of the best case of resistors design, without much difficulty. The output stability is as good as the traditional design. The waveform is identical to the one shown above.

In this design, the area and Monte Carlo distribution are highly dependent on each other. A smaller area means stronger requirement on the sizing of transistors, which lead to more manufacture variation, and vice versa. A too small design can lead to a sigma of around 10mV, which is 1000 times bigger than the one for the traditional design. But with reasonable sizing, the sigma can be pushed down below 1mV but the area will grow exponentially. In system design, if components of this manner are involved, a reference plot of sigma versus estimated area usually comes in handy. Designers can thus size the transistors based on the plot so that the variation stays just in the acceptable range. The author generated several reference plots and below is an example:

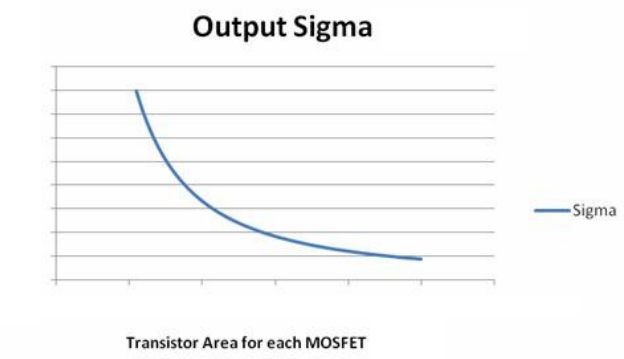

Figure 7: An example sigma-Area plot

The exact data were not supposed to be included but we can see from the plot that the curve converges to some asymptote limit. Hence this design sometimes might not be able to provide the robustness as needed. Also, the designers would not want to size the transistors at the area beyond the inflection point, because otherwise the design will not be very efficient on area.

With acceptable variation, the area of this design is on the order of 1000um^2, which is acceptable and also 10,000 times more efficient than the traditional design. The variation can be pushed down below 5mV with reasonable sizing, which is not as good but lies in acceptable range.

This design is extremely sensitive to temperature change. Simulation shows that a temperature of 100 C will make the Monte Carlo sigma shoot up from around 1mV to about 10mV, which is too much off the accepted range. This result is as disastrous as the area of resistor-in-series design because 100 C is not a rare condition for integrated circuits. Hence further measures must be taken to improve the robustness under high temperature.

C. Diode-Connected MOSFET Design

Generally, this design exhibits good functionality and performance under simulation. Thus this one is very likely the best choice.

The steady state current is extremely low because the transistor at the bottom of the stack barely has any voltage difference among source, gate and drain. The value is usually below 300fA and for the best case can be below 10fA, which is as much as noise consumes in the circuit. This design has no problem with output accuracy as well.

The area and Monte Carlo sigma are interdependent as well. An example sigma-area plot looks like follows.

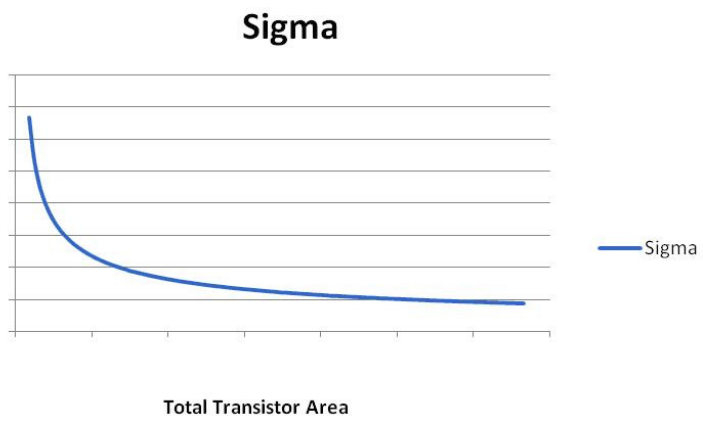

Figure 8: An example sigma-Area plot for the diode circuit

There are two main differences between the plot for the diode circuit and for the off-state MOS. First, the asymptote limit of off-state MOS is lower than of diode, which makes the former a better choice when higher accuracy is needed. However, the curve for diode circuit converges much faster to the limit than does the off-state MOS. For the same level of accuracy, diode circuit uses about only half of the area of off-state MOS design. The area needed to reach expected value is around 500um^2 versus around 1000um^2 for the off state MOS design.

Fortunately, this design appears not to be affected by temperature change at all. The simulation at 100C yields identical result with the one at 27C. This is not surprising because there are many identical devices involved in the circuit and they are all affected by variation in a almost perfectly random way. Hence, if there are enough devices, the variations cancel each other out. This feature makes the circuit practically more useful under various conditions.

D. Switched Capacitor Design

The last design is the most interesting but most complex one. Switched-Capacitor circuit is usually used for high power regulators but the group was seeking to use it in a low power environment by driving the circuit with slower clock.

An analysis to the first order shows that the average current can be below 10pA, which is desirable. But as the whole circuit switches, very high but narrow coupling current spikes appear and might be harmful to the source. The current spike can be around 100uA range. The plot below shows an example current profile.

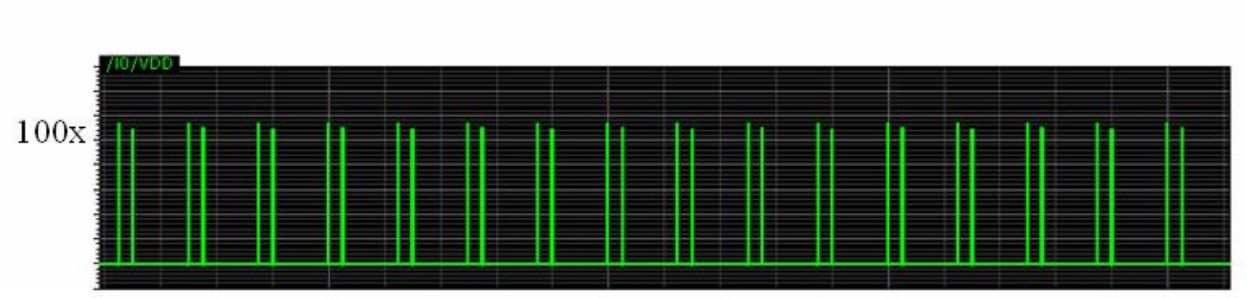

Figure 9: An example current spiking profile

Since the circuit is constantly switching, the output has to be oscillating as well because of the coupling effect. This phenomenon might severely affect the accuracy but techniques such as the use of dummy switches can suppress the oscillation and limit the magnitude within 1mV. Below are two plots showing the voltage waveforms with and without suppression measures.

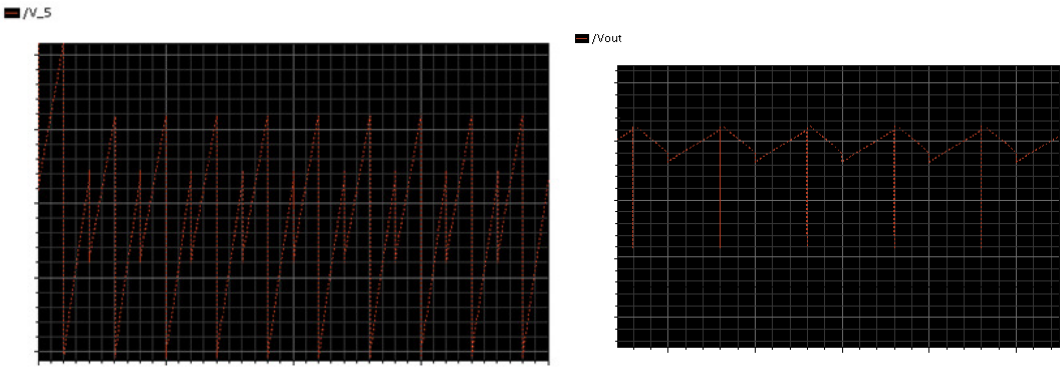

Figure 10 and 11: An example output waveform before(left) and after(right) suppression

The area of this design, including all the configurations overhead, is around 15000um^2, which is about 10 times bigger than the two MOSFET designs. Much of the area is devoted to the capacitors in order to stabilize the voltage distribution. In actual implementation, some technologies are able to re-use the area taken by the capacitors, and this design is thus still viable.

Monte Carlo simulations show that this design is robust at low temperature. The simulation usually gives a sigma around 1mV. However, this design fails at high temperature as well. At 100C, the sigma goes up to as high as 50mV. The reason still remains to be seen. Further analysis is needed to solve this problem.

IV. Future Work

This section introduces two further improvements that still remain to be done, besides solving the problems of the designs at high temperature. Both improvements are for the switched capacitors. Even though switched-capacitor design does not have as good performance as others based on the data we have, this design has much more potential than we have seen because people have rarely tried to use it for low current design.

In this section, we discuss two possible ways to enhance the design and hence make the comparison closer to completeness.

A. Low Current Switched Capacitor Design

This idea is used to solve the high current spike problem, as shown in Figure 8. An instantaneous high current spike is needed to turn either on or off the MOSFET, and the peak value sometimes can be around 100uA, which is beyond the upper limit of low-current power supply. Since the spikes are narrow, though high, the actual charge released from the supply is little. We can thus solve this problem using a virtual source. Below is a diagram of the design.

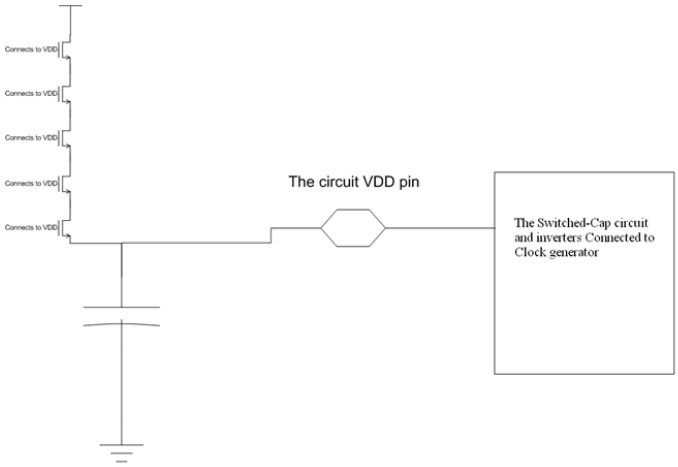

Figure 12: diagram of a virtual source design

In this design, we are supplying voltage using a capacitor and connect the real source to the capacitor through some high resistance. Thus all the spikes will come directly from the capacitor instead of the real source. Since the frequency of our circuit is extremely slow, the resistance connecting the virtual and real sources can be very high, so that some of the coupling power will be saved. Below is the current waveform of a first order simulation:

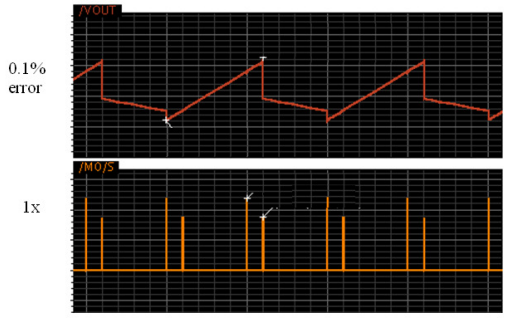

Figure13: lowered current spike and the output voltage

The diagram shows that the virtual source only caused 0.1% of deviation at the output, which is negligible. But the current spikes from the real source are reduced to only 1% of the original. This result is close but still out of our expected range.

For further improvement, we can even replace the resistance path with an off-state MOSFET, so that the current will be limited to extremely low, because the MOSFET can conduct only fA range current when off. Below is the improved design diagram:

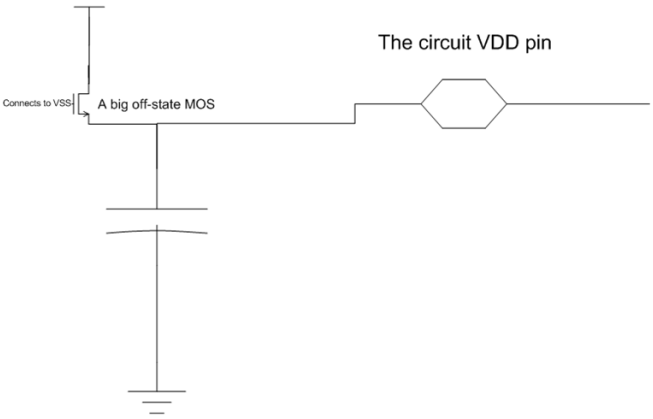

Figure 14: improved virtual source

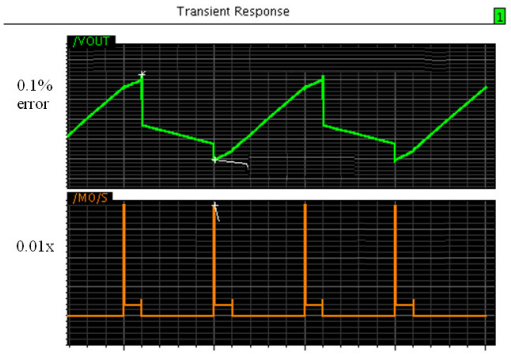

Figure15: Voltage and current waveform

The result turned out to be surprisingly good. The output still only has 0.1% error but the current was reduced(from 100x) to only 0.01% of the original value. If reliable, this makes the switched capacitor design even more power-efficient than the diode design.

All the results in this part, however, are only first order analysis. Further verifications of the design are needed because the result values were improved too much. But if the results prove valid, the switched capacitor design will have a great advantage at power saving.

B. A unified Switched Capacitor Models

Another advantage worth exploring is that the switched capacitor design might be tunable as well as the resistor design. Below is the design diagrams of dividing by 5, 6, 7 and 8 switched-capacitor circuits.

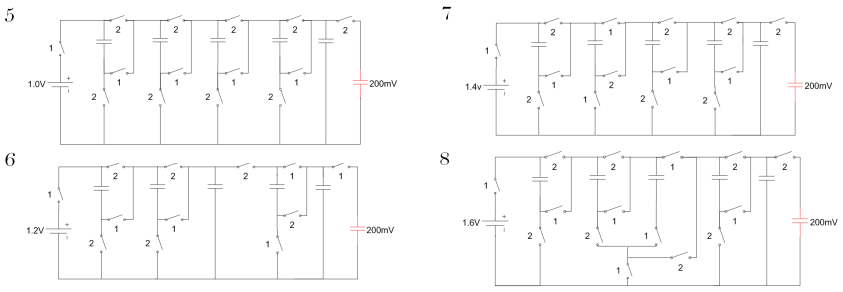

Figure16: diagrams of switched-capacitor designs

We can see from Figure 12 that the circuits have great similarities. Hence, with the same 5 capacitors, it is possible to develop a flexible divider that provides division by any number between 2 and 8, just by manipulating the clock signals through a controller. Nonetheless, this is still only an idea and its feasibility still remains to be seen in more experiment and actual implementation.

V. Conclusion

In this report we mainly discussed the pros and cons of 4 designs of low-current voltage dividers. The traditional resistors-in-series design is still the most reliable design but its size makes it impossible to realize. The off-state MOSFET design has desirable current and area but it fails at high temperature. The diode-connected circuit is the most robust after resistors, and it is generally not affected by temperature change. But the design involves many devices and might add to the complexity. The switched capacitor design provides correct functionality but does not have as good performance and efficiency as other designs. However, it has more potential to develop.

The most reasonable choice based on the presented data should be the diode-connected circuit because it is so far the most reliable among the realizable designs. But further studies might show switched-capacitor design better.

VI. Acknowledgement and Reference

a) Acknowledgement

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b) **Reference**

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